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The influence of wire cutting and selective etching conditions on the structural perfection of CdZnTe 211(B) substrate wafers

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The slicing of CdZnTe ingots using diamond wire cutting was investigated. Optimal process conditions were determined, enabling an increase of up to 30% in the number of wafers obtained from a single ingot compared to the diamond saw cutting method. It is shown that the use of selective etching after slicing allows for the visualization of the dislocation pattern and serves as a reliable method for rejecting substrate material at the early stages of the manufacturing process.

Keywords: cadmium-zinc-telluride (CdZnTe), semiconductor ingot, diamond wire cutting, selective etching.

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The cadmium-zinc-tellurium (CdZnTe, CZT) solid solution is one of the most demanded materials in modern microelectronics. Device wafers based on it are used in the production of infrared (IR) array photodetectors as a substrate material for epitaxial structures of mercury-cadmium-tellurium (HgCdTe, MCT), as well as in X-ray detectors [1, 2]. The main disadvantage of this material is its high cost and limited production volumes, which stem from the specific features of grown CZT ingots, including a block structure, the presence of dislocations and other structural imperfections. Furthermore, the labor-intensive processing technology results in a low yield of acceptable wafers due to the low hardness and high brittleness of the material [3]. Increasing the yield of acceptable wafers at all

stages of production of CdZnTe substrate wafers is an urgent task aimed at improving the availability of IR devices based on HgCdTe/CdZnTe heterostructures.

One of the fundamental process operations is the slicing of a large-block CZT ingot into wafers. The structural features of the grown ingots do not allow for slicing parallel to their base, as is typical for other semiconductor materials, which imposes limitations on the process methods used [4]. The most well-established and commonly used method for separating CZT ingots into wafers remains slicing with a diamond inner cutting blade (DICB). The cutting tool is a metal disc with a central hole and a diamond-based abrasive material applied on its edge (Fig. 1a). This DICB, specially mounted in

a drum and rotating at a speed of 3000–5000 rpm, slices the ingot at an average speed of 40–50 mm/min (Fig. 1b). After slicing off each wafer, the mechanism returns the ingot to its original position, moves it by a specified step, and the cycle repeats.

When a large-block CdZnTe ingot is sliced using a DICB, the thickness of the cut blank wafer is about 2000 μm , which is necessitated by the brittleness of the CZT material. A reduced in thickness of the cut wafer increases the risk of mechanical fracture, which likely occurs due to micro-vibration of the DICB during slicing. After wafers are separated from the ingot by blade cutting, a typical pattern with a “rounded” morphology is observed on the surface (Fig. a),

and the depth of the damaged near-surface layer is about 100 μm on each side of the cut wafer, taking into account the physical and mechanical features of the CZT material [5]. Investigation of a typical surface pattern of a CZT wafer sliced with a DICB shows a height variation of 25–35 μm (Fig. 2b).

Considering the depth of the damaged layer after such slicing, at least 300 μm in total is removed from both sides of the blank wafer during further processing operations. Subsequent grinding/polishing operations reduce the wafer thickness to the required $900 \pm 100 \mu\text{m}$. Thus, material losses during the operations following the DICB slicing alone amount to more than half of the cut wafer thickness.

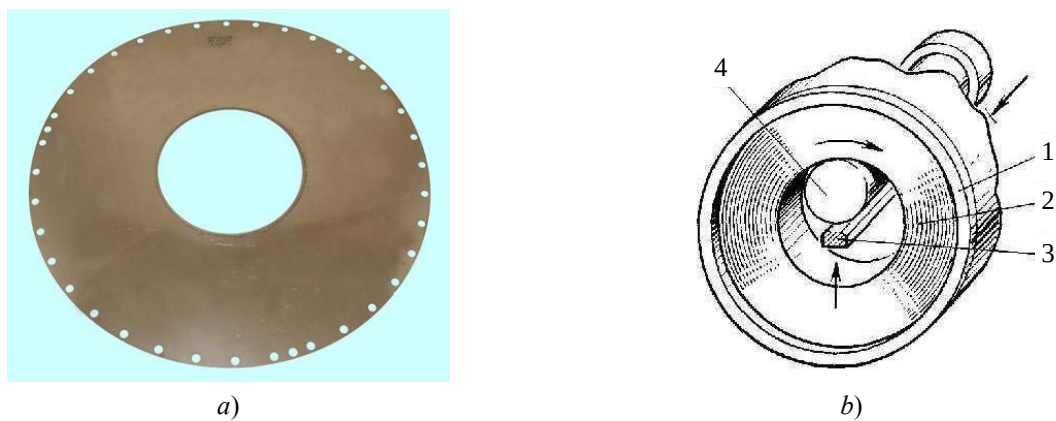


Fig. 1. Diamond inner cutting blade with peripheral mounting holes (a) and ingot slicing scheme (b), where 1 – cylindrical drum; 2 – DICB; 3 – mandrel holder; 4 – ingot

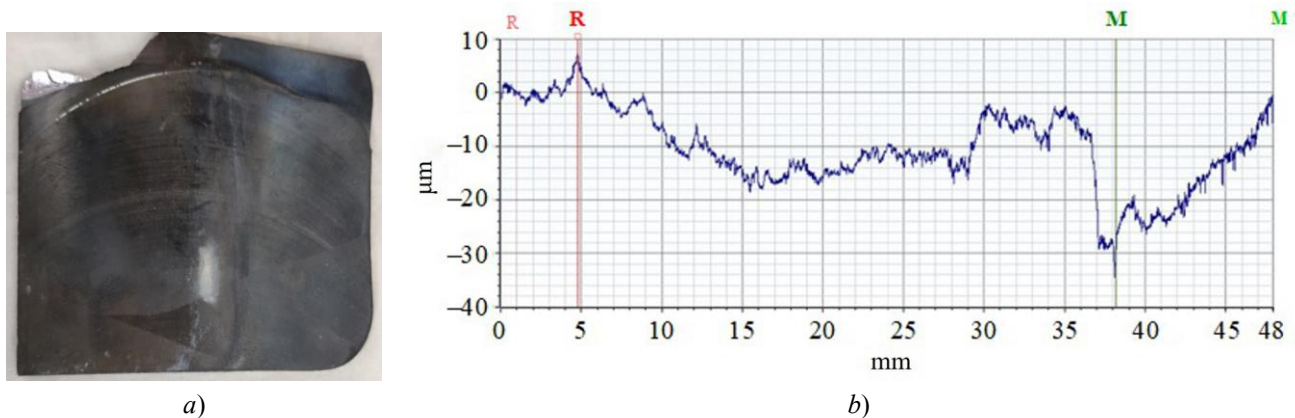


Fig. 2. Surface of a CdZnTe wafer after DICB slicing: a) – appearance of the wafer; b) – measurement of the surface pattern using a contact profilometer

The next generation in the evolution of methods for slicing semiconductor ingots into wafer blanks is the wire slicing method (with diamond-coated wire or with an additional supply of abrasive material into the cutting zone). The main advantages of this method (Fig. 3) are the use of a wire with a relatively smaller diameter compared to the thickness of a DICB, which allows for reduction in the kerf width and, consequently, minimizes material losses during slicing. Furthermore, the natural damping provided by the wire flexibility reduces thermodynamic loads, which in turn reduces the damaged layer thickness. This allows for the slicing of thinner wafers, thereby increasing the yield of wafers obtained from a single ingot.

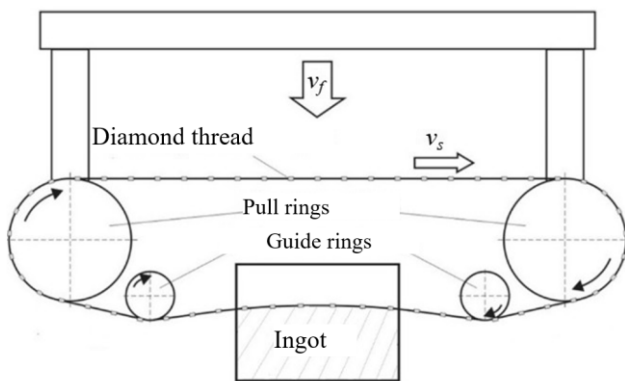


Fig. 3. Schematic diagram of the wire slicing setup

However, to exploit the above-mentioned advantages of the diamond wire slicing method, it is necessary to determine the optimal process conditions (e.g., ingot feed rate, wire drum rotation speed, cooling fluid supply, etc.), while considering the mechanical and structural features of the semiconductor material being processed.

Furthermore, one of the aspects affecting process productivity is the mounting of the ingot on the coordinate table of the slicing setup. The criteria for selecting a mounting material include rapid hardening, easy release from the wafer/ingot, and the ability to maintain shape during slicing despite minor vibrations and a continuous flow of water.

As a result of research and analysis of various mounting materials, the following combination was identified: gypsum is used for creating a mold and fixing a sample on the coordinate table of the slicing setup, and a cyanoacrylate adhesive is applied at the contact points between the semiconductor ingot and the gypsum. This combination of materials withstands the impact of water both as a flow and during immersion. This allowed mounting of the sample on the coordinate table of the slicing setup steadily and to control over the process of separating the ingot into wafers (Fig. 4).

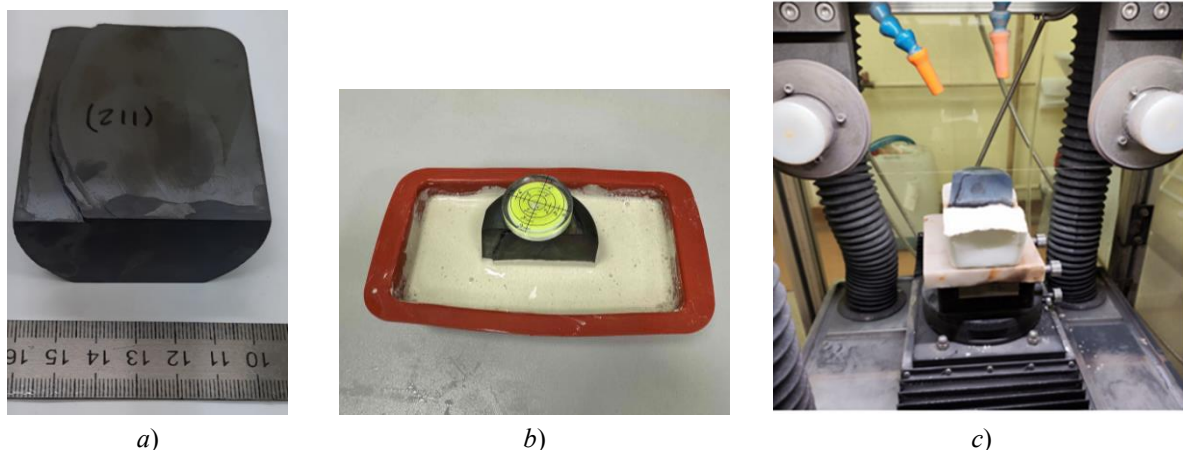


Fig. 4. Large-block CdZnTe ingot: a) – oriented in direction (211); b) – in a special retaining mold; c) – secured on the coordinate table of the slicing setup and ready for separation into wafers

The use of diamond wire for slicing a large-block CZT ingot allowed reducing the thickness of the processed wafers down to 1400 μm without loss of mechanical strength (Fig. 5). The suitability of such wafers for further

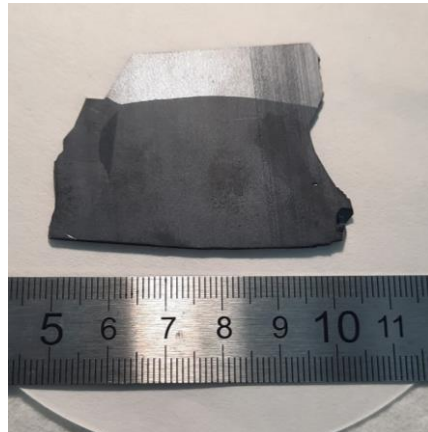
grinding/polishing operations was confirmed at subsequent processing stages.

The surface morphology of CZT wafers sliced by the diamond wire slicing method was also studied using the contact profilometry

(Fig. 6). The height variation is less than $20\text{ }\mu\text{m}$, which does not exceed the same parameter for wafers sliced with a DICD.

To assess the depth of the near-surface damaged layer on a CZT wafer after diamond

wire slicing using various process approaches to optimize slicing conditions, the lateral cleavage edge of the wafer was studied using the scanning electron microscopy (Fig. 7).



a)



b)

Fig. 5. CdZnTe wafer cut by diamond wire slicing method: a) – appearance of the wafer; b) – thickness measurement using a digital micrometer

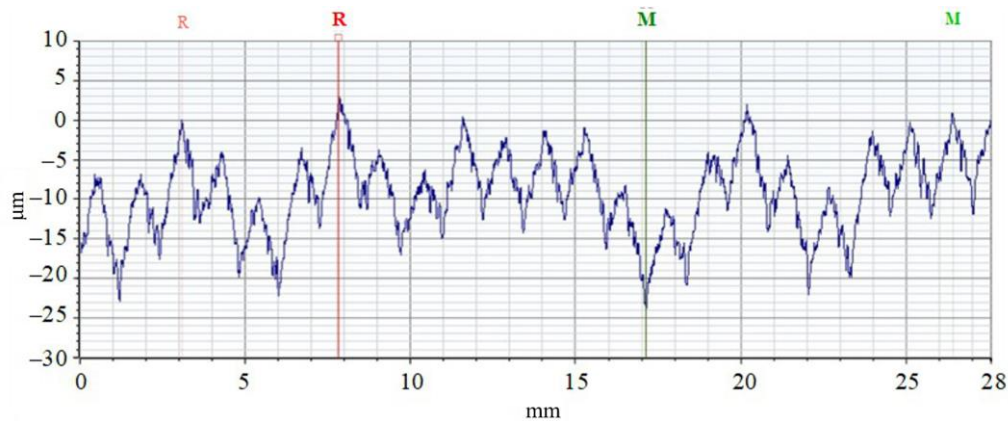


Fig. 6. Surface pattern of a wafer sliced using diamond wire

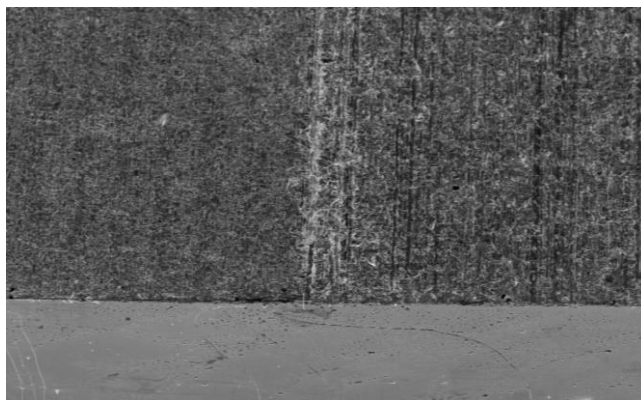


Fig. 7. General view of the investigated wafer fragment at an angle of 40°

In Fig. 7, the interface between the processed areas in a more optimal (left) and non-optimal (right) mode can be clearly seen.

More detailed examination of the near-surface damaged area assessed the damaged layer depth

at the level of $10\text{--}15\text{ }\mu\text{m}$ under optimal slicing conditions (Fig. 8a) and of about $40\text{--}50\text{ }\mu\text{m}$ under non-optimal conditions (Fig. 8b), which confirms the importance of properly selecting the process parameters for this operation.

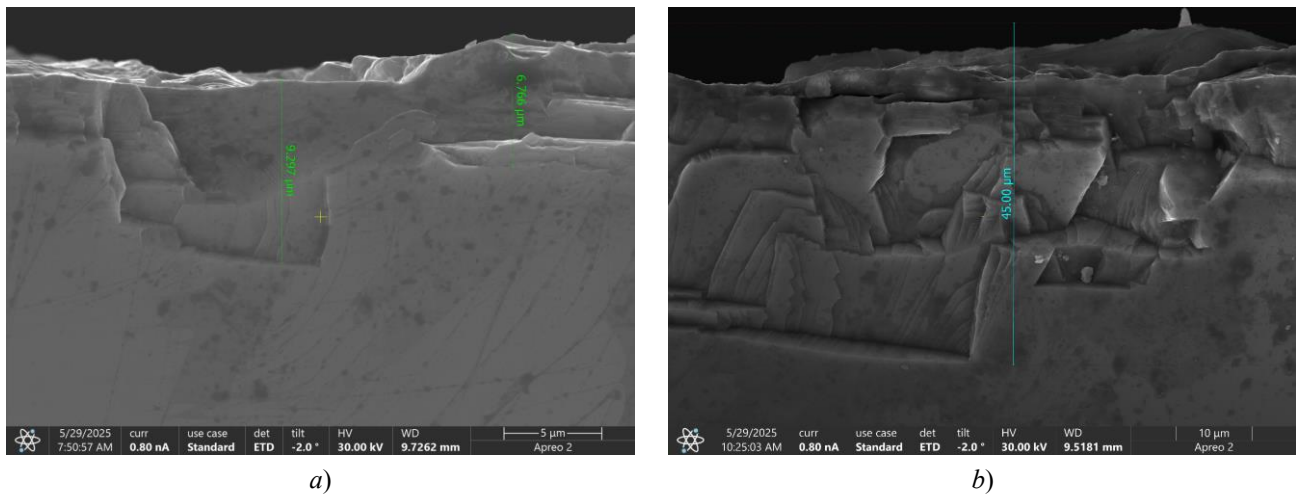


Fig. 8. Investigation of the near-surface damaged layer depth of a CZT wafer after diamond wire slicing:
a) – area under optimal slicing conditions; b) – area under non-optimal slicing conditions

Thus, the study of possible applications of diamond wire slicing for separating large-block CZT ingot and determination of process conditions allowed for a reduction in the thickness of the cut wafers, the height variation of the wafer surface pattern, and the depth of the resulting near-surface damaged layer. Combined, these improvements reduce overall material losses and increase the yield of usable wafers at this stage as compared to DICB slicing.

Then, the sliced wafers undergo defect structure analysis to determine the single-crystalline region, block structure, and/or twinning over the wafer area, identify the A/B sides and count the dislocation density. Specific features of the material under consideration include its pronounced softness, low critical shear stress, and low stacking fault energy, which result in relatively easy dislocation generation during crystallization in the ingot growth process [6]. Dislocations in the crystal lattice of the material have a direct impact on the quality of epitaxial structures grown thereon. While defects caused by mechanical processing at the slicing and grinding stages can be minimized by subsequent polishing, growth defects extend throughout the entire depth of the material. Detection of a wafer's non-compliance with structural requirements at this production stage allows for its rejecting it in due time, thus preventing obviously unsuitable samples from proceeding to

the labor-intensive processes of subsequent mechanical and chemical-mechanical processing, as well as epitaxial growth, thereby reducing costs and increasing the yield of usable devices [7].

One of the optimal methods for revealing the dislocation pattern in substrates is selective chemical etching. In addition to dislocations, this technique allows for the visualization of twins and block structures, thereby helping to identify the single-crystalline region and determine the polarity of the wafer sides, which is important for future growth processes. Since the anisotropy of the crystal properties need accounting for during the development of selective etching, the etchant is selected based on the crystallographic orientation of the wafers under study. To reveal the dislocation pattern and determine the polarity of wafers with a (211)B orientation, Everson's solution was used [8]. Prior to the selective etching process, it is necessary to remove the damaged layer formed after ingot separation into wafers, which is achieved by chemical-mechanical polishing of the wafer on both sides.

A specific pattern becomes visible on the wafer after selective etching, allowing for the determination of the polarity (sides A/B) of the single-crystalline region, blocks, and twins (Fig. 9). Side A acquires a matte-dark color due to cadmium (Cd) enrichment, whereas side B has a metallic luster due to tellurium (Te).



Fig. 9. Appearance of a CdZnTe wafer (211)B after selective etching. The contour marks the single-crystalline region on side B of the cut wafer section

After selective etching, optical microscopy is used to analyze the wafer surface in the marked region on side B to determine the dislocation density. Dislocation pits have an asymmetric shape with a clearly defined pointed apex (Fig. 10) due to the deviation of the plane of the crystallographic orientation under consideration (211) from the reference plane (111) by 19.5° , which induces anisotropy in the pit projection on the surface. Pits with round or irregular contours lacking a pronounced apex do not originate from dislocations (for example, they represent tellurium precipitates or artifacts of mechanical processing) and are not counted in the calculation. If they significantly distort the overall pattern, they can be studied separately.

To estimate the dislocation density value correctly, measurements are taken over several equally spaced fields, followed by calculation of the average value. The optimal number of fields is selected depending on the size of the marked region. The edge zone with a width of 2-3 mm is excluded from consideration, since the defect density in it is systematically higher due to the contact of the melt with the crucible walls during crystal growth, while peripheral areas of the substrate are generally not involved in formation of active elements during manufacture of array photodetectors.



Fig. 10. Typical view of the dislocation pattern of the single-crystalline region of a CdZnTe wafer (211)B after selective etching

The criterion of suitability for the epitaxial growth of HgCdTe during the fabrication of IR devices is a value of not more than $3 \times 10^4 \text{ cm}^{-2}$ [9, 10]. During the study, the dislocation density was calculated on the substrate wafers sliced by the method considered herein. It was established that the samples meet this criterion, which allowed to conclude that they are suitable for further processing operations.

Conclusion

Thus, the application of the considered process solutions optimizes the manufacturing process of CdZnTe wafers (211)B. Compared to slicing with a DICB, the separation of large-block CZT ingots into wafers using the diamond wire slicing method allows for the slicing of thinner ($1400 \mu\text{m}$ vs $2000 \mu\text{m}$) blank wafers with a shallower damaged layer, while maintaining wafer integrity. This increases the number of wafers obtained from a single ingot by up to 30% and also reduces the subsequent processing time.

Selective etching to reveal the spatial non-uniformity of defect distribution, followed by the dislocation density calculation, allows for assessing the suitability of the wafer for subsequent epitaxial growth operations, thereby facilitating the early rejection of unsuitable samples and establishing a basis for reproducible incoming qualification of substrates.

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